CLAIMS

1. An apparatus for performing an emulation of an electronic circuit and for transmitting and receiving, via a network, packets conveying data relating to the emulation, the apparatus comprising:

a circuit board;

at least one emulation resource mounted on the circuit board, each for emulating a behavior of at least a portion of the electronic circuit by producing output signals in response to input signals in a manner controlled by input programming data; and

a network/resource interface circuit mounted on the circuit board for transmitting input signals to the at least one emulation resource, the input signals being of states controlled by data conveyed by packets arriving via the network, and for transmitting on the network packets conveying data representing states of output signals produced by the at least one emulation resource.

2. The apparatus in accordance with claim 1 further comprising:

random access memory (RAM) mounted on the circuit board, wherein the network/resource interface circuit stores data representing states of output signals produced by the at least one emulation resource in the RAM during the emulation and thereafter transmits on the network packets conveying the data it stored in the RAM.

3. The apparatus in accordance with claim 1 further comprising:

random access memory (RAM) mounted on the circuit board, wherein the network/resource interface circuit stores data conveyed by packets arriving via the network in the RAM prior to performing the emulation, and then controls states of inputs signals it transmits to the at least one emulation resource in response to the data it stored in the RAM.

4. The apparatus in accordance with claim 1 wherein the network/resource interface circuit also supplies data conveyed by packets received via the network as the input programming data to the at least one emulation resource.

5. The apparatus in accordance with claim 1 wherein the at least one emulation resource comprises a plurality of programmable logic devices (PLDs), each having a plurality of terminals for

receiving its input signals and for transmitting its output signals, and wherein the apparatus further comprises:

a first plurality of signal paths formed on the circuit board linking a first subset of the terminals of each PLD to terminals of others of the PLDs for conveying their output signals to one another.

6. The apparatus in accordance with claim 5 wherein each PLD comprises a field programmable gate array (FPGA).

7. The apparatus in accordance with claim 5 further comprising:

a bus, formed on the circuit board and connected in parallel to a second subset of the terminals of each PLD, for conveying input and output signals between each PLD and the network/resource interface circuit.

8. The apparatus in accordance with claim 5

wherein the network/resource interface circuit generates at least one clock signal, and

wherein the apparatus further comprises:

a clock bus connected between the network/resource interface circuit and each PLD, for concurrently delivering edges of the at least one clock signal to each PLD for clocking logic circuits within the PLDs during the emulation.

9. The apparatus in accordance with claim 8 wherein the network/resource interface circuit generates edges of the at least one clock signal in response to packets received via the network.

10. The apparatus in accordance wherein claim 8 wherein the network/resource interface circuit receives a primary clock signal generated external to the apparatus and generates edges of the at least one clock signal in response to edges of the primary clock signal.

11. The apparatus in accordance wherein claim 8 further comprising:

an oscillator mounted on the circuit board for generating a primary clock signal, wherein the network/resource interface circuit generates edges of the at least one clock signal in response to edges of the primary clock signal

12. The apparatus in accordance with claim 8 further comprising conductors mounted on the circuit board for conveying at least output signal of each PLD as a clock gating signal input to the network/resource interface circuit, wherein the network/resource interface circuit generates the at least one clock signal as a function of a clock gating signal received from at least one of the PLDs.

13. The apparatus in accordance with claim 5 further comprising:

a plurality of cable connectors, each corresponding to a separate one of the PLDs, and

signal paths coupling each cable connector to a second portion of the terminals of its corresponding PLD.

14. The apparatus in accordance with claim 5 further comprising:

a plurality of random access memories (RAMs), each corresponding to a separate one of the PLDs, and

signal paths coupling each RAM to a second portion of the terminals of its corresponding PLD such that each PLD can read and write access it when programmed to do so.

15. The apparatus in accordance with claim 5 further comprising:

a plurality of cable connectors, each corresponding to a separate of the PLDs,

signal paths coupling each cable connector to a second portion of the terminals of its corresponding PLD,

a plurality of random access memories (RAMs), each corresponding to a separate one of the PLDs, and

a plurality of switches (S1-S8), each corresponding to a separate one of the RAMs, each selectively coupling the corresponding RAM to the second portion of the terminals of the PLD corresponding to that RAM such that when coupled to its corresponding RAM, each PLD can read and write access it when programmed to do so.

16. The apparatus in accordance with claim 15 wherein the network/resource interface circuit controls the plurality of switches in response to data conveyed in packets received via the network.

17. The apparatus in accordance with claim 6

wherein the network/resource interface circuit generates at least one clock signal,

wherein the apparatus further comprises:

a local bus, formed on the circuit board and connected in parallel to a second subset of the terminals of each FPGA, for conveying input and output signals between each FPGA and the network/resource interface circuit;

a clock bus mounted on the circuit board for concurrently delivering edges of the at least one clock signal to each FPGA for clocking logic circuits within the PLDs during the emulation; and

conductors mounted on the circuit board for conveying at least output signal of each FPGA as a clock gating signal input to the network/resource interface circuit, wherein the network/resource interface circuits generates the at least one clock signal as a function of a clock gating signal received from at least one of the FPGAs.

18. The apparatus in accordance with claim 17 further comprising:

a plurality of cable connectors, each corresponding to a separate of the FPGA s;

signal paths coupling each cable connector to a second portion of the terminals of its corresponding FPGA;

a plurality of random access memories (RAMs), each corresponding to a separate one of the FPGA s; and

a plurality of switches, each corresponding to a separate one of the RAMs, each selectively coupling the corresponding RAM to the second portion of the terminals of the FPGA corresponding to that RAM such that when coupled to its corresponding RAM, each FPGA can read and write access it when programmed to do so., wherein the network/resource interface circuit controls the plurality of switches in response to data conveyed in packets received via the network.

19. The apparatus in accordance with claim 17 wherein the network/resource interface circuit generates edges of the at least one clock signal in response to packets received via the network.

20. The apparatus in accordance wherein claim 17 wherein the network/resource interface circuit receives a primary clock signal

generated external to the apparatus and generates edges of the at least one clock signal in response to edges of the primary clock signal.

21. The apparatus in accordance wherein claim 17 further comprising:

an oscillator mounted on the circuit board for generating a primary clock signal, wherein the network/resource interface circuit generates edges of the at least one clock signal in response to edges of the primary clock signal.

22. The apparatus in accordance with claim 17 further comprising:

random access memory (RAM) mounted on the circuit board, wherein the network/resource interface circuit stores data conveyed by packets arriving via the network in the RAM prior to performing the emulation, and then controls states of inputs signals it transmits to the at least one emulation resource in response to the data it stored in the RAM.

23. The apparatus in accordance with claim 17 further comprising:

random access memory (RAM) mounted on the circuit board, wherein the network/resource interface circuit stores data representing states of output signals produced by the at least one emulation resource in the RAM during the emulation and thereafter transmits on the network packets conveying the data it stored in the RAM.

24. The apparatus in accordance with claim 15 further comprising:

another switch (S9) for selectively interconnecting signal paths between the second portion of the terminals of at least two of the PLDs.